AMENDMENTS TO THE CLAIMS

1. (Currently amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in the device set A sending data to one or more nodes in the node set T;

a device set Z mutually exclusive of the node set T with each device in the device set Z receiving data from one or more nodes in the node set T; and

a collection C of node subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C such that:

for a device x in the device set Z, a sequence $cx = cx_0, cx_1, cx_2, \ldots, cx_J$ exists with each member of the sequence cx being a node set in the collection C, the sequence cx passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message directly from a device in the device set A being a member of node set cx_L and a node of the path R that sends data directly to the device x being a member of node set cx_V with U being larger than V;

for a member Y of the collection C, a corresponding set of devices Z(Y) exists in the device set Z such that a device y is included in the set of devices Z(Y) only if the member Y is also a member of a sequence cy;

for members cx_H and cx_K of the sequence cx with $H > K$, a device set $Z(cx_K)$ is a subset of a device set $Z(cx_H)$;

the sequence cx includes two members cx_L and cx_m with L>M and with a device set $Z(cx_M)$ being a subset of a device set $Z(cx_L)$ and a device exists in the device set $Z(cx_L)$ that is not included in the device set $Z(cx_M)$; and

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the node set T includes three distinct nodes p, q, and r, the node p being in a member cx_D of the sequence cx, the nodes q and r being in a member cx_E of the sequence cx with D > E, in one path of the plurality of paths P(x) a message moves directly from the node p to the node r and in another path of the plurality of paths P(x) a message moves directly from the node q to the node r.

2. (Original): An interconnect structure according to Claim 1 wherein:

the plurality of paths of the sequence cx include a path such that if a message hops from a node in a member cx_n to a node in a member cx_m, then n > m.

3. (Previously presented): An interconnect structure according to Claim 1 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets $LV = LV_0, LV_1, \ldots LV_J$, each member of the hierarchy LV being a node set that is subset of the node set T and each node in the node set T is contained in exactly one member of the node sets LV; and

for the device x of the device set Z, a node set cx_N is a subset of a level N node set L_N, with N not exceeding J.

4. (Previously presented): An interconnect structure according to Claim 3 wherein:

the collection C includes 2^{J-N} members on a level N;

the collection C includes three members D, E and F such that member node set D is on a level LV_N and member node sets E and F are on a level LV_{N-1};

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the node set D to the node set F; and

the device set Z includes device sets Z(D), Z(E), and Z(F) that correspond to the three members D, E, and F, the device sets Z(E) and Z(F) being mutually exclusive device sets, and the device set Z(D) is the union of the device sets Z(E) and Z(F).

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5. (Previously presented): An interconnect structure according to Claim 1 further comprising:

a logic L_p associated with the node p wherein for a message Mp that arrives at the node p, the logic Lp uses information concerning the sending of messages from the node q for the logic Lp to determine where the node p is to send the message Mp.

6. (Previously presented): An interconnect structure according to Claim 1 wherein:

the node q has priority over the node p to send data to the node r so that a message Mq located at the node q is not blocked from being sent to the node r by a message Mp at the node p; and

the node q sends a control signal to the node p wherein the purpose of the control signal is to enforce the priority of the node q over the node p to send data to the node r.

7. (Previously presented): An interconnect structure according to Claim 1 wherein:

the node set T includes a node s distinct from the nodes p, q, and r, the node s being in the member cx_D, so that in one path of the plurality of paths P(x), a message moves from the node p directly to the node s.

8-13. (Canceled).

14. (Previously presented): An interconnect structure comprising:

a plurality of nodes including a node N_E and a node set P, the node set P including a plurality of nodes that send data to the node N_E; and

a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in pairs, a node pair including a sending node and a receiving node, the sending node sending data to the receiving node;

the nodes in the node set P having a priority relationship for sending data to the node N_E, the nodes in the node set P including distinct nodes N_F and N_A, the node N_F having a highest priority among the nodes in the node set P for

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sending data to the node N_E so that a message M_F arriving at the node N_F is not blocked from traveling to the node N_E by a message M_A arriving at the node N_A; and

for a message M arriving at the node N_A and the message M is blocked from being sent to the node N_E, then the blocking of the message M from being sent to the node N_E causes sending of the message M from the node N_A to a node distinct from the node N_E, wherein:

when a message M arrives at the node N_A and is targeted for the node N_E and not blocked by a message M' arriving at a node in the node set P having a higher priority than the node N_A for sending messages to the node N_E, the node N_A sends the message M to the node N_E.

15-23. (Canceled).

24. (Previously presented): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive with the node set T with each device in the device set A sending data to a node in the node set T;

a device set Z mutually exclusive with the node set T with each device in the device set Z receiving data from a node in the node set T;

a set of data paths P, each path of the path set P carrying data from a device in the device set A to a device in the device set Z, each node on the path of the path set P is included in the node set T, and each interconnect in the path is included in the interconnect set I;

a node set U characterized as the set of nodes within the node set T that are on a path included in the path set P;

for a node N in the node set T such that the node N is on a path in the path set P, a corresponding set of devices Z(N) exists in the device set Z such that a device w is included in the device set Z(N) only if a path exists in the path set P from a member of the device set A to the device w such that the path contains the node N;

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the node set U includes three distinct nodes N_A, N_D, and N_E such that the node N_A sends data to the node N_D and the node N_E, and a device set $Z(N_A)$ is the same as a device set $Z(N_D)$, and a device set $Z(N_E)$ is a proper subset of the device set $Z(N_A)$;

an interconnect link IL in interconnect set I, the interconnect link IL being an interconnect link on a path in the path set P such that a corresponding set of devices Z(IL) exists in the device set Z such that a device w is included in the device set Z(IL) only if a path containing the interconnect link IL in the path set P exists from a device in the device set A to the device w; and

the node set U includes distinct nodes N_A, N_D, and N_E such that the node N_A sends data to the node N_D on a link L_{AD}, the node N_A sends data to the node N_E on a link L_{AE}, and a device set $Z(L_{AE})$ is a proper subset of a device subset $Z(L_{AD})$.

25-35. (Canceled).

36. (Previously presented): An interconnect structure S comprising:

a plurality of nodes including nodes N_A, N_D, and N_E;

a plurality of interconnect lines selectively coupling the nodes in the structure S;

a plurality of devices in a device set I that is mutually exclusive of the plurality of nodes, the devices in the device set I sending data to one or more of the plurality of nodes; and

a plurality of devices in a device set Z that is mutually exclusive of the plurality of nodes, the devices in the device set Z receiving data from one or more of the plurality of nodes, the device set Z comprising a plurality of device subsets further comprising:

a device subset T_A consisting of devices t_A such that a message can be sent from a device in the device set I through the node N_A to the devices t_A;

a device subset T_D consisting of devices t_D such that a message can be sent from a device in the device set I through the node N_D to the devices t_D; and

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a device subset T_E consisting of devices t_E such that a message can be sent from a device in the device set I through the node N_E to the devices t_E;

wherein:

the node N_A sends data to the node N_D;

the node N_A sends data to the node N_E;

the devices in the device subset T_A are included in the device subset T_D; and

a device t_A exists that is included in the device subset T_A and excluded from the device subset T_E.

37. (Previously presented): An interconnect structure S according to Claim 36 further comprising:

a logic L that controls passage of messages sent through the interconnect structure S, wherein:

a plurality of messages P can be sent to a plurality of nodes from a plurality of devices in the device set I;

the plurality of messages P includes a message M_A having a target device in the device subset T_A; and

the logic L routs the message M_A through the node N_A to a device in the device subset T_A.

38. (Previously presented): An interconnect structure S according to Claim 37 wherein:

the message M_A has a header; and

the logic L routs the message M_A through the interconnect structure S using information in the header of the message M_A.

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39. (Currently amended): An interconnect structure S according to ~~Claim 36~~ Claim 37 wherein:

the logic L is distributed among one or more nodes of the plurality of nodes;

the plurality of nodes includes a node N; and

logic of the logic L associated with the node N uses control signals to route messages through the node N.

40. (Previously presented): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T including three distinct nodes N_A, N_D, and N_E;

a device set I mutually exclusive of the node set T and containing devices that send data to at least one node in the node set T;

a device set Z mutually exclusive of the node set T and containing devices that receive data from at least one node in the node set T;

a plurality of paths P that carry data through the interconnect structure S to devices in the device set Z;

a device subset T_A exists such that a message can be sent on a path in the paths P from a device in the device set I through the node N_A to a device in the device subset T_A;

a device subset T_D exists such that a message can be sent on a path in the paths P from a device in the device set I through the node N_D to a device in the device subset T_D;

a device subset T_E exists such that a message can be sent on a path in the paths P from a device in the device set I through the node N_E to a device in the device subset T_E;

wherein:

the node N_A sends data to the node N_D along a path in the paths P;

the node N_A sends data to the node N_E along a path in the paths P;

the devices in the device subset T_A are included in the device subset T_D; and

a device exists that is included in the device subset T_A that is not included in the device subset T_E.

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41. (Original): An interconnect structure S according to Claim 40 further comprising:

a logic L_A associated with the node N_A controls data flow from the node N_A.

42. (Previously presented): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T including three distinct nodes N_A, N_C, and N_E;

a device set I mutually exclusive of the node set T and containing devices that send data to at least one node in the node set T;

a device set Z mutually exclusive of the node set T and containing devices that receive data from at least one node in the node set T;

a plurality of paths P that carry data through the interconnect structure S to devices in the device set Z;

a device subset T_A exists such that a message can be sent on a path in the paths P from a device in the device set I through the node N_A to a device in the device subset T_A;

a device subset T_C exists such that a message can be sent on a path in the paths P from a device in the device set I through the node N_C to a device in the device subset T_C;

a device subset T_E exists such that a message can be sent on a path in the paths P from a device in the device set I through the node N_E to a device in the device subset T_E;

wherein:

the node N_C sends data to the node N_E along a path in the paths P;

the node N_A sends data to the node N_E along a path in the paths P;

the devices in the device subset T_C are included in the device subset T_E; and

a device exists that is included in the device subset T_A that is not included in the device subset T_E.

43. (Original): An interconnect structure S according to Claim 42 further comprising:

a logic L_A associated with the node N_A controls data flow from the node N_A.

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44. (Original): An interconnect structure S according to Claim 43 wherein:

a message M arriving at the node N_A has a header and the logic L_A uses information in the header to decide where to send the message M.

45. (Original): An interconnect structure S according to Claim 43 wherein: the logic L_A uses information from the node N_C to decide where to send the message M.

46-70. (Canceled).

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